Test and performances of the engineering model of PICsIT, the high energy detector plane on board the INTEGRAL satellite

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ABSTRACT

IBIS (Imager on Board INTEGRAL Satellite) is a space-telescope designed to produce sky images in the 15 keV to 10 MeV energy range with an angular resolution of several arcminutes over a wide field of view. This is obtained by deconvolving the shadowgram projected by a coded mask onto two pixellated detector layers sensitive to the incident radiation interaction position. The upper layer, ISGRI (INTEGRAL Soft Gamma-Ray Imager), consists of 16384 CdTe elements operating in the low energy range (15 to 600 keV), while the underlying layer, PICsIT (Pixellated Imaging CsI Telescope), is made up of 8 identical modules housing altogether 4096 CsI(Tl) scintillating crystals coupled to PIN photodiodes operating in the 0.15 to 10 MeV energy range. The expected performances of IBIS were described in a dedicated session of the SPIE Symposium in August 1996, while performances of the PICsIT single detection units have been presented at SPIE in July 1998.
The analog front-end electronics has a direct impact on performances in terms of lower energy threshold, energy resolution and event time tagging, thus it is one of the most critical parts of a detector. In PICsIT, an analog-digital custom-made ASIC, that manages signals coming from 16 detecting units has been designed. Three of them have been used in the Engineering Model (EM) in order to check the instrument behaviour by means of a reduced prototype comprising a module with 32 detection units, the ancillary electronics and a test equipment. The main goal of these tests was the evaluation of:
- scientific data processing methods and scientific data transmission on a high bit rate line
- detector qualification parameters and telemetry / telecommand functionality on a low bit rate line

The EM was the first fully representative model of the PICsIT system. Although in a reduced version it was the benchmark of the various components, such as the ASIC or the host PCB, whose behaviour was tested and analysed in great detail. The knowledge of PICsIT achieved with the EM has driven the design improvements that will be implemented for the Qualification Model that will be built before the final realisation of the Flight Instrument.
This paper describes the architecture of PICsIT as it is in the current EM configuration and its test equipment. The main results on system functionality will also be presented, while greater detail on the scientific performances achievable is available in another paper presented at this conference [1]

Keyword: INTEGRAL, IBIS, PICsIT, Photodiodes, CsI(Tl) crystals

1. INTRODUCTION

The International Gamma-Ray Astrophysics Laboratory (INTEGRAL) is a gamma-ray telescope generating high resolution spectroscopy and wide-field imaging with fine angular resolution.
IBIS (Imager on Board INTEGRAL Satellite) is one of the two main scientific instruments on the INTEGRAL payload with its imaging and spectroscopy capability. The detector features two superimposed planes: the upper one, ISGRI (Integral Soft Gamma-Ray Imager), consist of 8 identical modules of 512 polycells, each containing 4 CdTe detectors, while the lower one, PICsIT (Pixelated Imaging CsI Telescope), is made of 8 identical modules each housing 512 CsI(Tl) scintillating crystals viewed by PIN photodiodes. The design provides a high degree of modularity and the CsI(Tl) modules have the same cross-sectional shape as those of the CdTe. A tungsten coded mask is optimised for high angular resolution and a thin lead passive shield, covering the distance between the mask and CdTe detection plane, restricts the detector aperture for the soft gamma-ray part of the spectrum. An active BGO scintillator veto system shields the detector bottom as well as the four sides up to the bottom of CdTe plane.

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2. PICsIT GENERAL DESCRIPTION

The Pixellated Imaging Caesium Iodide Telescope (PICsIT), shown in the blocks diagram of fig. 1, is composed of the detector plane, two dedicated PICsIT Electronic Boxes (PEB1 and PEB2) and the related harness up to the Hardware Event Pre-processing Interface (HEPI) that is the first board of the IBIS Data Processing Electronics boxes (I_DPE1 and I_DPE2) that interface ISGRI and PICsIT to the satellite On Board Data Handling (OBDH) system.
The detector plane consists of 8 rectangular modules (PDMs, from PICsIT Detector Modules), each one integrated into a stand-alone testable sub-system. Each module consists of 512 square CsI(Tl) crystal bars and associated front-end electronics boards. Each CsI(Tl) bar is optically coupled to a custom-made low leakage silicon PIN photodiode to allow for conversion of light pulses in charge pulses. With this configuration the design provides a high degree of modularity.

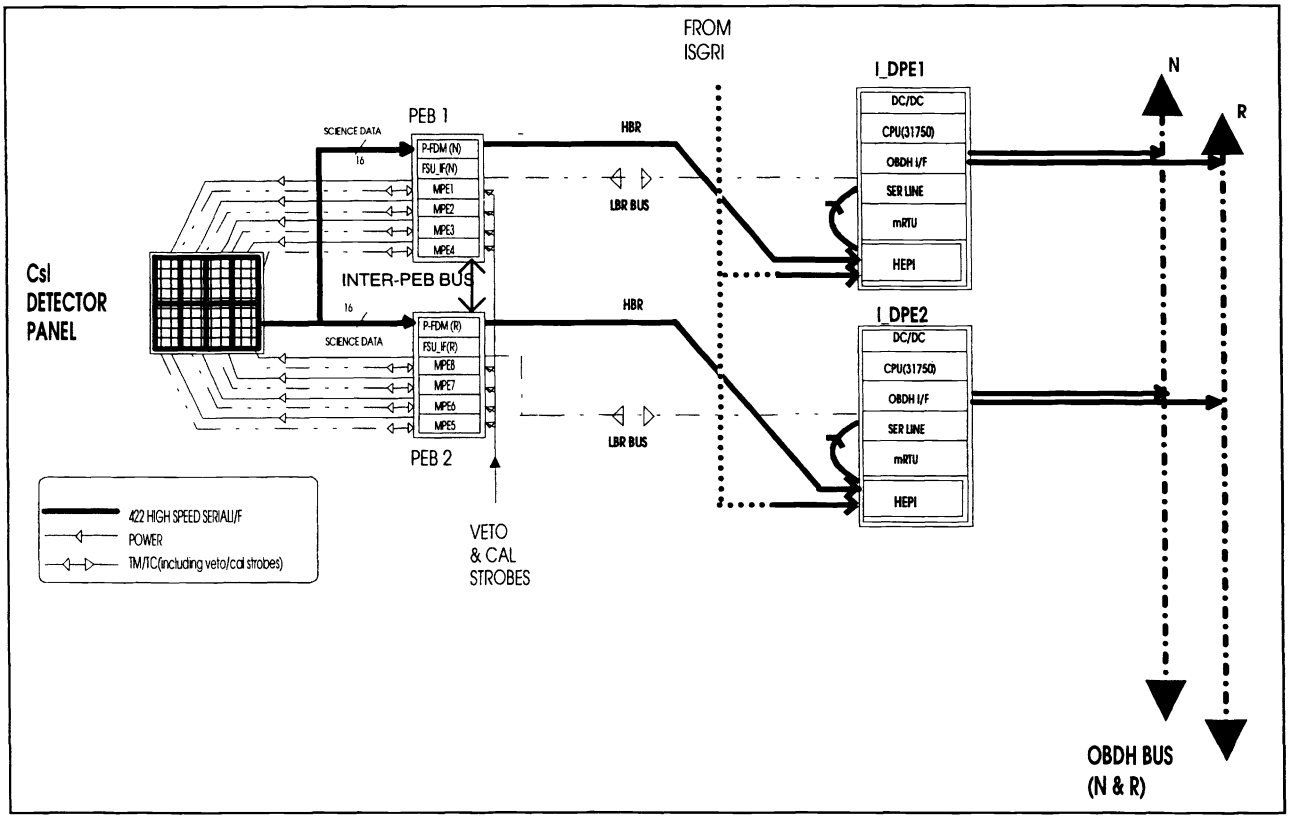

Fig. 1 PICsIT block diagram

For each module (Fig. 2) a mechanical egg-crate structure houses the scintillator crystal/Photodiode unit, and gives mechanical support to the module electronics. In each module there are three Printed Circuit Boards (PCBs) placed below the crystals/PDs. The module electronics is able to interface the PDs and to process the information of their signals up to the Analog to Digital (A/D) conversion.
PICsIT also encompasses two external units, PEB1 and PEB2 (PICsIT Electronics Box). These electronic boxes carry the DC/DC converters for the eight modules, as well as the circuits for sorting all the CsI(Tl) events coming from different modules according to their arrival time. This last function, the sorting, is performed by hardware logic in the FIFO Data Management board (P_FDM). The PEB boxes include a low-speed, microcontroller-based, communication network for House-Keeping (HK) and Telecommand (TC) data exchange with IBIS-DPE.
Data collected from PICsIT are sent to the IBIS_Digital Processing Electronic (I_DPE) boxes for data processing passing through a Hardware Event Pre-processor Interface (HEPI) that is a board physically placed inside the I_DPEs. For the scientific data transmission, a High Bit Rate (HBR) serial interface, running at 4 Mbps, is provided from PICsIT to HEPI. House-keeping (HK) and Telecommands (TC) to/from PICsIT are routed via a Low Bit Rate (LBR) serial interface running at 16Kbit/sec.

3. MODULE DESCRIPTION

Each of the 512 CsI(Tl) crystals in a module has an 8.55x8.55 mm square cross-section and is 30 mm thick. A photodiode is glued on one of the two square sides. The crystal is surrounded by a light diffusive coating and it is inserted into an aluminium mechanical structure with 512 positioning holes, the egg-crate, whose mechanical tolerances determine the positioning precision of the crystals. When a crystal is hit by a gamma-ray, it creates light photons that are collected by the photodiodes and converted into charge pulses. Information are derived, into AFEE and DFEE, from signal amplitude, time of arrival and crystal position.
Each detector module (fig. 2) is provided with three Printed Circuit Boards, they are (from top to bottom):

1) Photo Diodes (PDs) biasing distribution board
2) Analogue Front End Electronics (AFEE) board
3) Digital Front End Electronics (DFEE) board

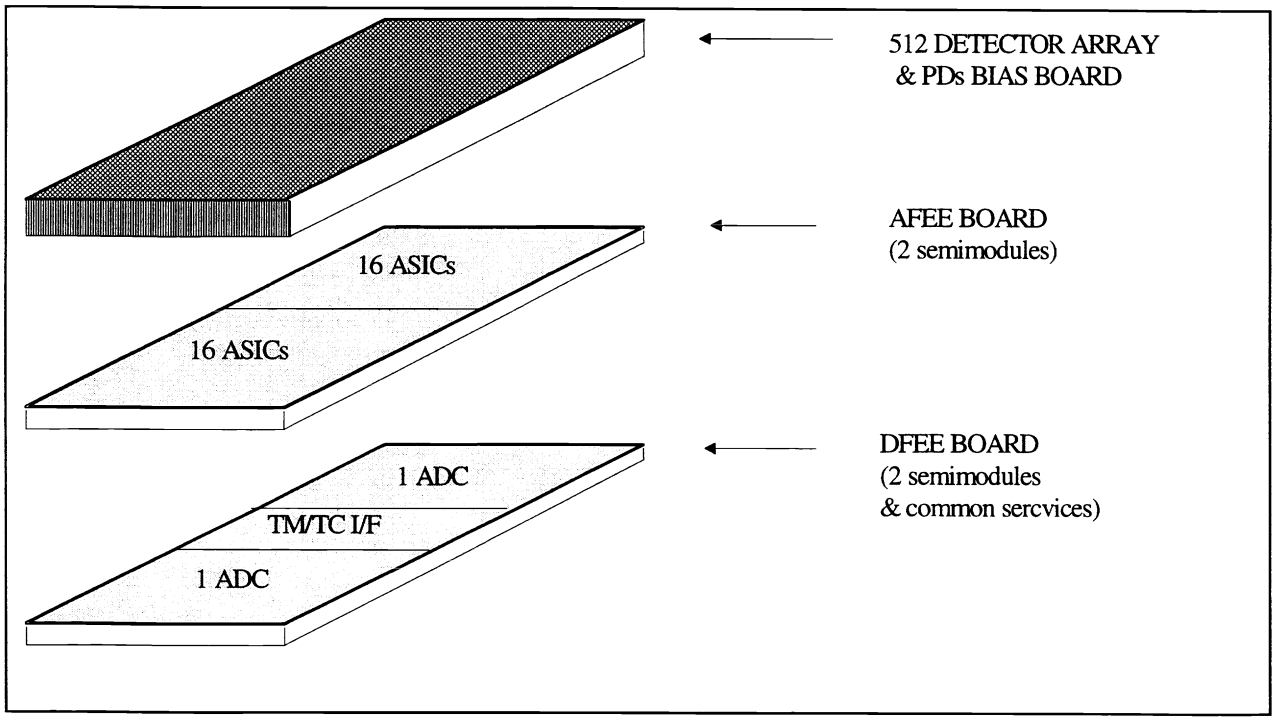

Fig. 2 PICsIT module assembly

The PDs are soldered to the first PCB that simply hosts all the required biasing filters and includes the paths for a proper routing of the PD signals to the lower AFEE board.

The second PCB (AFEE) houses 32 identical Application Specific Integrated Circuits (ASICs) that are the core of the analogue analysis of the PD signals and determine the performance of the whole instrument in terms of energy threshold, energy resolution and time tagging precision of the events.

The ICARUS ASIC [2], shown in fig. 3, serves 16 PDs and includes for each channel the following main circuits:
- the stages of charge conversion and shaping amplification
- self-triggering circuitry via an amplitude discriminator
- peak detector with analogue storage of the peak level
- an anti-coincidence controlled by an external veto signal

Moreover, the ASICs include a 16 channel analog multiplexer with a sparse read-out logic and some important ancillary functions such as threshold setting, killing of noisy channels and threshold auto-calibration.

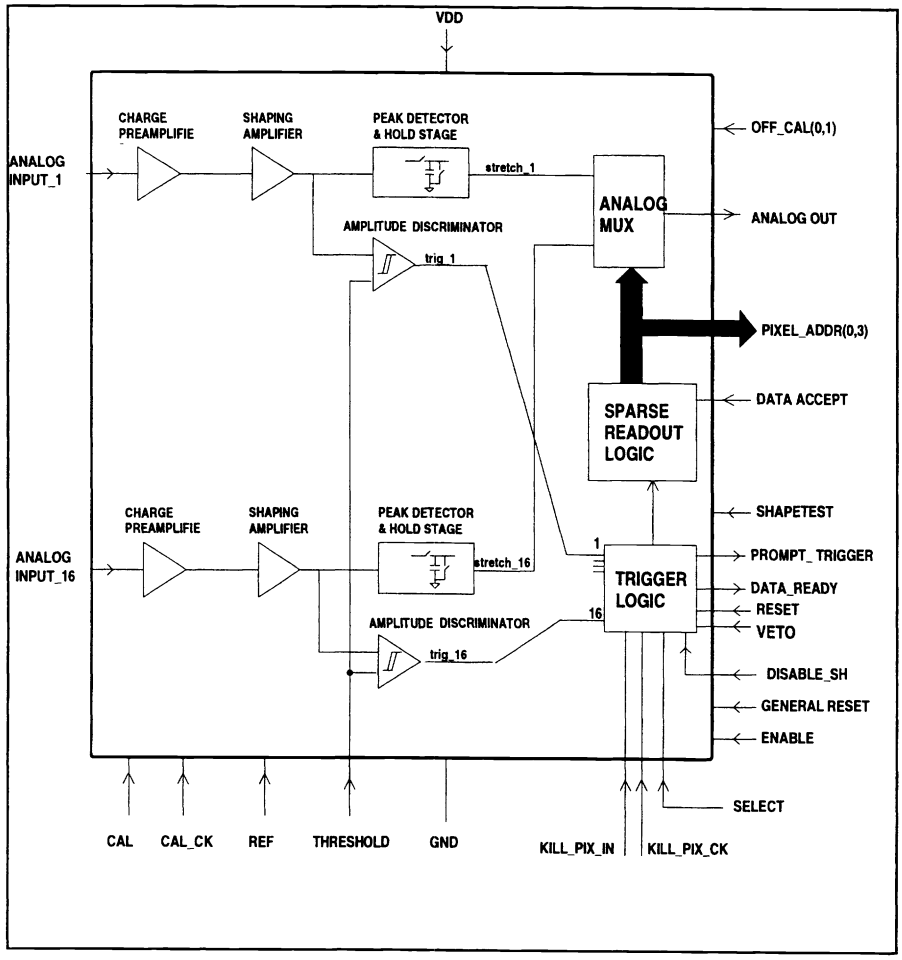

Fig. 3 ASIC schematic diagram

The third PCB (DFEE) is placed just under the AFEE board and is connected to it via a dedicated harness. The DFEE includes two identical processing chains (semimodules), each of them managing the data collection from 16 AFEE ASICs (or 256 PD channels); this division of tasks has been implemented in order to reduce the data processing time.
Each section of the DFEE will be able to perform the following functions:

- interface with 16 ASICs of its related AFEE board
- detect a "Data Ready" signal from the ASICs indicating an event has occurred
- assign a "time mark" to the event
- identify the ASIC (one or more) which generated the "Data Ready" and perform an A/D conversion of the pulse level stored in the "active" pixels
- pixel address identification
- reset if more than three "active" pixels are found and flag the event
- manage a coincidence check with the IBIS tagged calibration source and flagging of the event
- format output data in a 48 bit word (containing event time, pixel address, pulse amplitude, flags)
- temporarily store output data in a local FIFO
- manage serial transmission of output data to the P_FDM
- provide a rate-meter of events detected by the semimodule it is serving.
- provide a live time meter related to its "busy" time.

Also each DFEE will be in charge of ancillary functions, implemented by a unique circuit for the whole module, related to power and house-keeping control, rate metering of relevant strobe signals and telecommand executions. For a typical gamma-ray photon that interacts in two elements of a module the processing time will be less than 30 μsec.

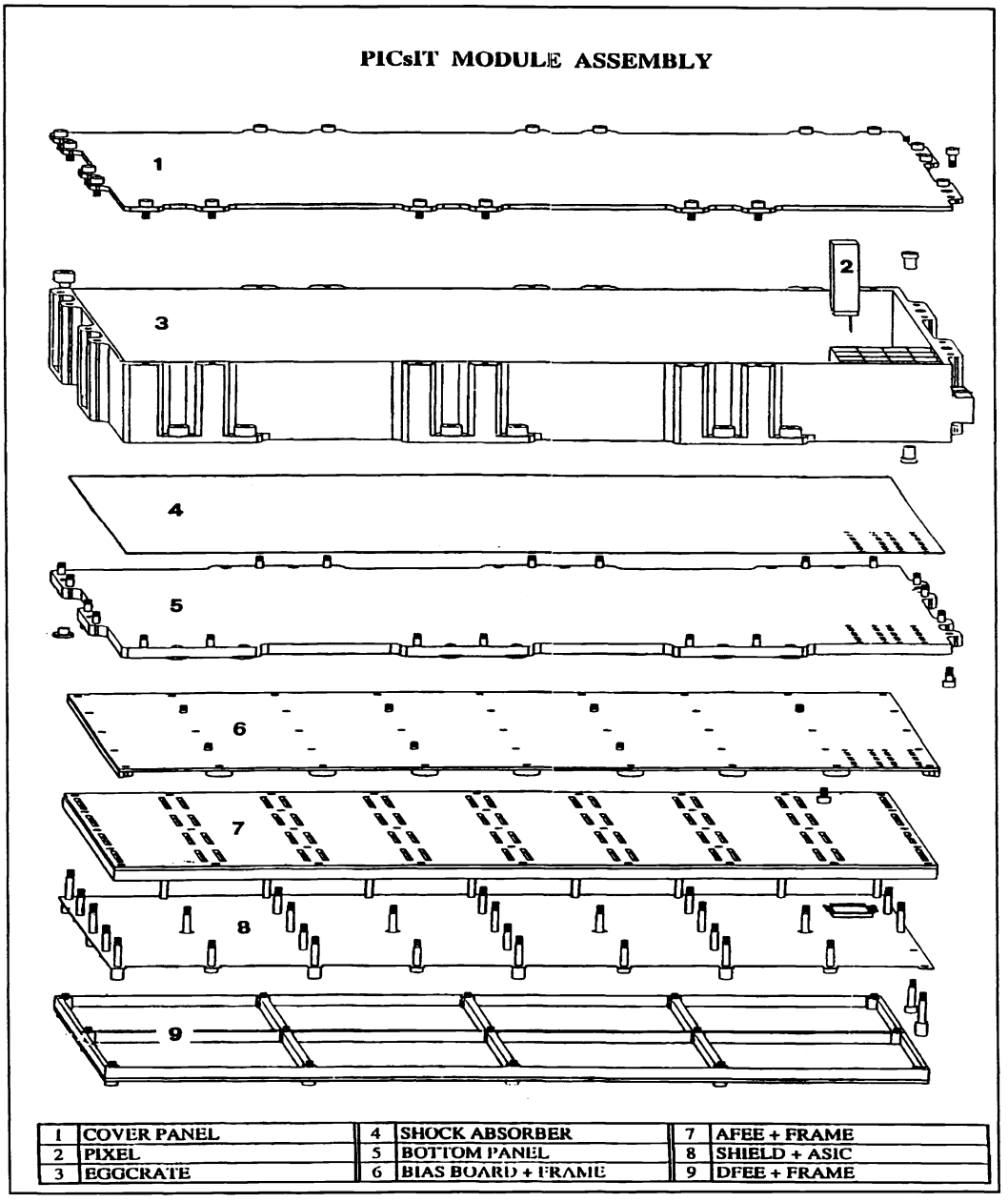

Fig. 4 Exploded view of the module structure.

4. ELECTRONICS BOX DESCRIPTION

The PICsIT detector plane is interfaced to the other subsystem of IBIS by means of two PICsIT Electronics Boxes (PEB1 and PEB2). Each PEB is composed of the following main elements (fig. 1):

- One PICsIT FIFO Data Manager Board (P_FDM) that may be Nominal or Redundant. The P_FDM collects the event data from all16 semimodule output FIFO's, their ordering "by time of arrival", their proper formatting, their storage into a FIFO for further transmission to the HEPI board via a High Bit Rate (HBR) serial link.
- One Microcontroller Board (FSU_IF Nominal or Redundant) that is in charge of the full command handling, via a Low Bit Rate interface.
- Four DC/DC converter, each of them in charge of the supply of a given module: the PEB1 carries the DC/DC converters of the module 1,2,3 and 4, while the PEB2 carries the DC/DC converters of the modules 5,6,7 and 8.

Data from the PEBs are collected by two (Nominal and Redundant) I_DPE (IBIS_Data Processing Electronics) which provide an I/F with the On Board Data Handling bus. In particular the scientific data are collected for a first processing by the Hardware Event Pre-processor Interface (HEPI). The two PICsIT microcontrollers, one in each PEB, are in cold redundancy and the switching between them is out of the PICsIT control. The software and, in particular, the commands directed to PICsIT, are transparent to the microcontroller active at that moment. The system will always act as an I_DPE slave and it will communicate with I_DPE through the LBR on request.
Two logical parts constitute the PICsIT software: the *basic software* and the *application software*. From the operational point of view these two programs each correspond one to one operative mode: the *standby* and the *nominal* mode. Both programs interface the I_DPE for receiving commands and/or exchanging data through the Low Bit Rate link. The *basic software* performs all preliminary operations and low level functions on the memories. The application performs the full command handling, acquires and formats the housekeeping data, handles the table that contains all the relevant information of the detector (threshold levels, map of killed pixels, etc), monitors some parameters, changes operating mode and generates messages in case of alarm situations.

5. PICsIT ENGINEERING MODEL

The rationale of the Engineering Model (EM) was to build an instrument that is fully representative of the flight model from a technological and electrical point of view; this philosophy has been applied to the whole IBIS instrument thus allowing the testing of the interfaces of all its sub-system including PICsIT. Furthermore, for what concern PICsIT, the EM has been used as a benchmark for testing the parts of the technical design that were thought to affect the whole PICsIT performance. To fulfil these objectives the PICsIT EM was composed of a single detector module in a configuration reduced (but fully operative) and one electronics box (PEB). The EM test campaign was also the occasion to build, prove and use a dedicated PICsIT Test Equipment. For the EM the PDM egg-crate contained only 32 bars positioned in one corner of the module as shown in fig. 5, so there are only 3 ASICs in the AFEE, while the DFEE was fully representative of the Flight Model (FM).

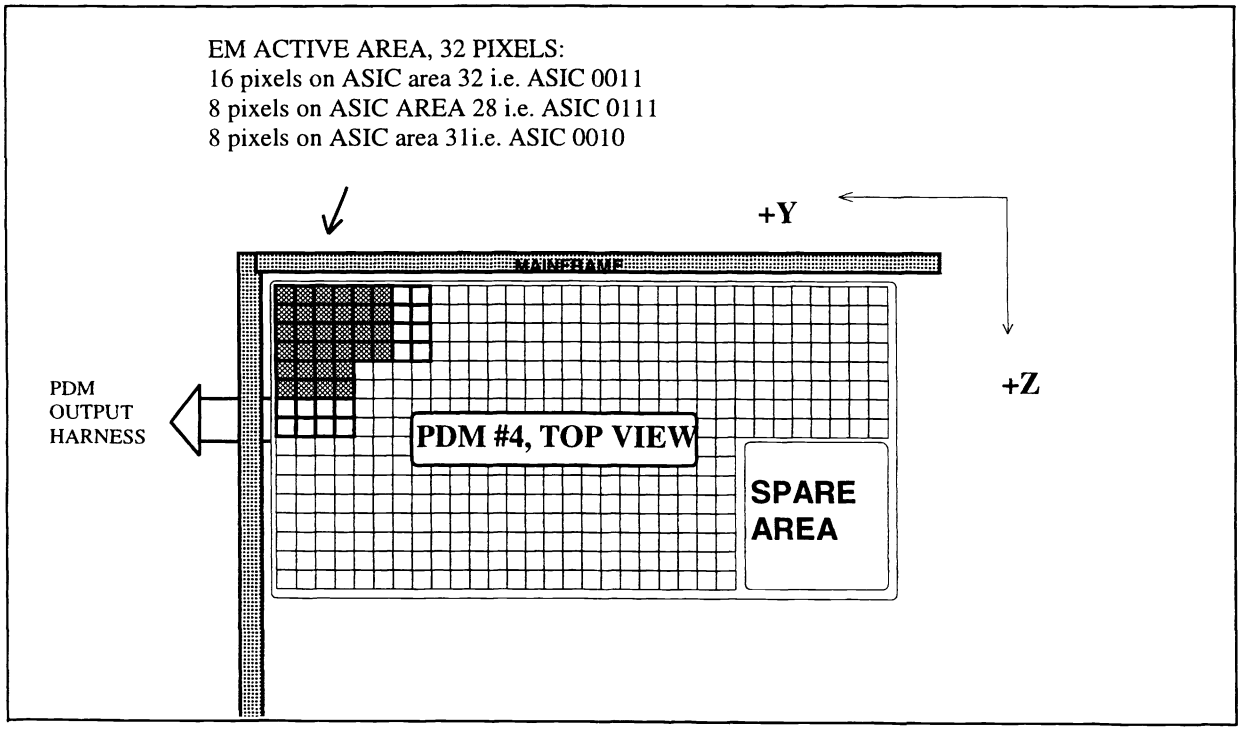

Fig. 5 Schematic of the module EM detectors position

The PEB comprised the FIFO Data Management (P_FDM), the micro-controller board (FSU_IF) and just one Module Power Electronics (MPE) for the PDM under test. The PICsIT Test Equipment, as shown in fig. 6, consists of a Central Check-Out Equipment (CCOE) which is used to send telecommands to the instrument and to the Science Test Equipment

(STE). Data acquired from the detector by the CCOE are distributed to the PICsIT Science Console (SC), where they are archived in raw format, and where is also possible to verify the correct functionality of the system in real time by using the Quick Look (QL) analysis SW.

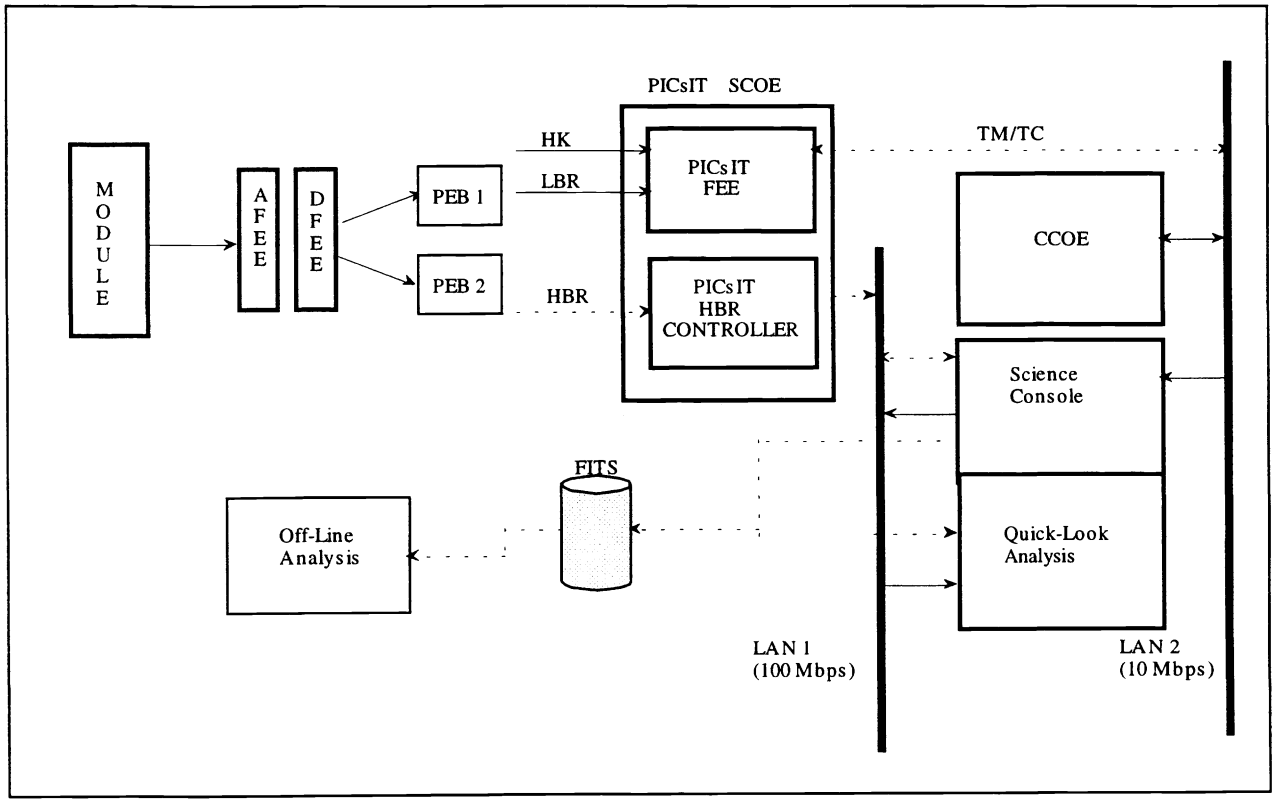

Fig. 6 PICsIT Test Equipment

The tests on the PICsIT EM were performed at LABEN laboratories in Milan. A long set of functional tests were performed in order to verify the entire system starting from the functionality of the Test Equipment and of all electrical interfaces, telemetry and telecommands.. The correct digital treatment of the data was tested and during this phase one of the 32 pixels was found to be noisier than average, a fault later found to be dependent on the layout of the AFEE board that picked up some noise from the DFEE; this noisy pixel was therefore killed during the tests.
Fig. 7 shows the ^{22}Na spectra measured by the 31 pixels of PICsIT EM from the off line analysis of the data.

6. CONCLUSIONS

No problem arose from the functionality point of view of the electronics systems, but the performances in terms of lower energy threshold and energy resolution are worse than expected from laboratory measurements previously performed on a single CsI(Tl) bar [4]. This is mainly due to cross-coupling between the analog and digital signals in the ASIC layout on the AFEE board and to a greater equivalent noise analog output from the ASIC itself (950 instead of the 800 e^-_{rms}). With a new design of the AFEE and a better screening of the ASICs to be used for the next Qualification Model (QM) it may be possible to reach a lower energy threshold of 150 keV instead of the currentl 200 keV and an energy resolution nearer 10% instead of 12.5% average measured here.

ACKNOWLEDGMENTS

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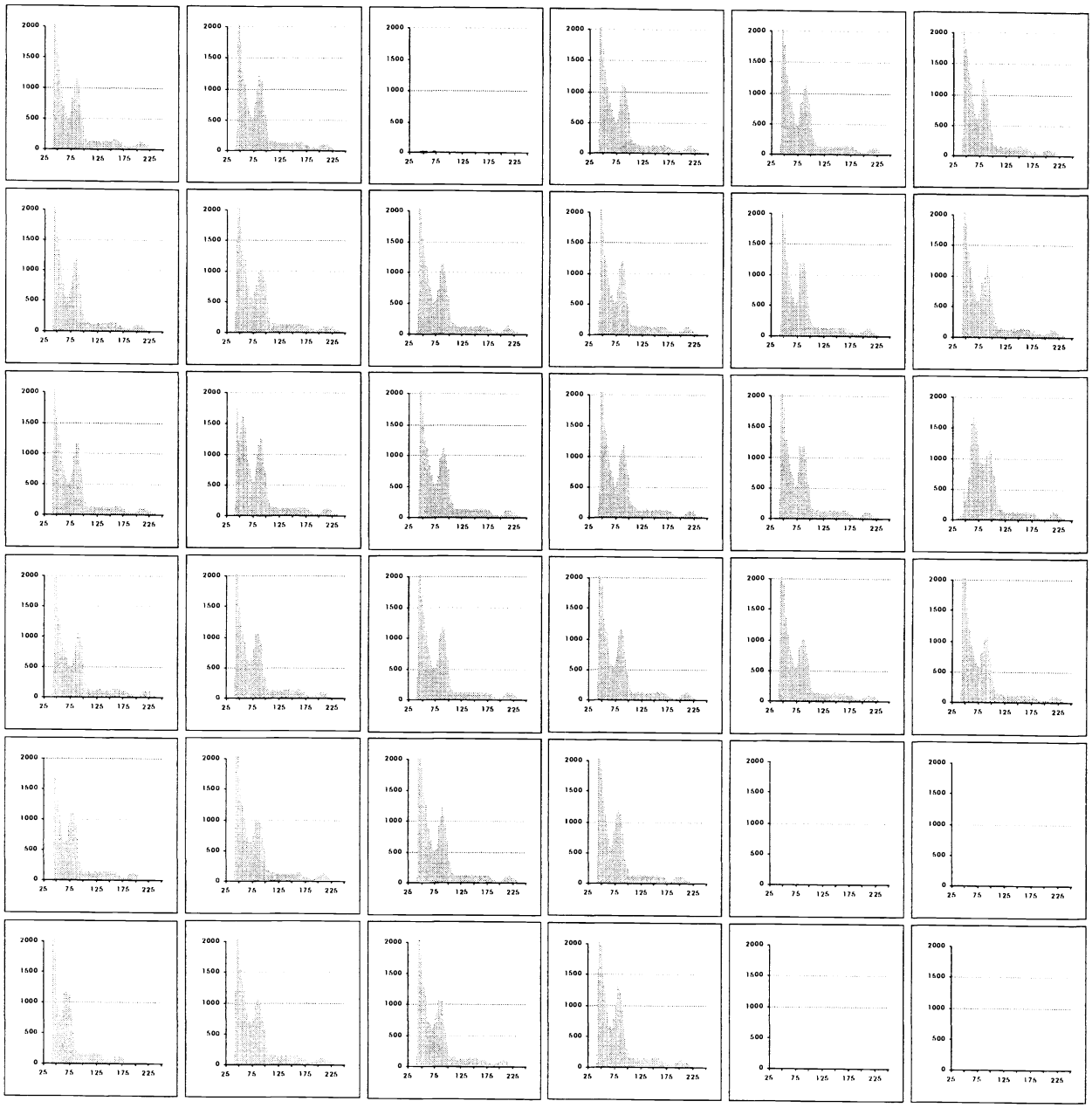

Fig. 7 Spectra of the PICsIT EM pixels irradiated with a ^{22}Na source.

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