

PICsIT: the high energy detection plane of the IBIS instrument onboard INTEGRAL

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ABSTRACT

IBIS is one of the two main instruments onboard the INTEGRAL gamma-ray satellite. IBIS will produce images of the gamma-ray sky in the region between 15 keV and 10 MeV by means of a coded mask coupled to a double-layer position sensitive detector.

PICsIT is the detection layer optimized for high energy. It has a total area of 3065 cm² and is composed by 4096 individual pixels made of CsI(Tl) crystal, each one with its proper electronic chain. The single units are 0.75 cm² in area, and 3 cm thick.

The front end electronics is designed so that analogue circuits, with their low noise figure, will allow the exploitation of the spectroscopic characteristics of the detector. The digital circuits will allow PICsIT to operate in anticoincidence with an active shield, and to deliver the interaction time of occurrence of the events.

Keywords: space instrumentation, gamma-ray detector, scintillators

1. INTRODUCTION

IBIS¹ (Imager onBoard INTEGRAL Satellite) is one of the two main instruments which will form the payload of the next ESA gamma-ray observatory satellite INTEGRAL (INTErnational Gamma-Ray Astrophysics Laboratory) due to be launched in the year 2001. IBIS will provide images with few arcminute resolution, over a wide field of view with a continuous spectral coverage from 15 keV up to 10 MeV.

The scientific requirements of IBIS are to achieve, at the same time, good continuum sensitivity and fine angular resolution. In designing a satellite-borne gamma-ray telescope with such characteristics, one should also bear in mind the limits of weight, volume and power consumption given by the mission scenario (IBIS mass limit = 648 kg, maximum power = 220 W).

The design of IBIS has therefore been based on an instrument having: a) Good detection efficiency over the 15-10000 keV energy range; this has implied the use of two separate detectors. One, ISGRI² (INTEGRAL Soft Gamma-Ray Imager), made of CdTe elements for low energy, and the other, PICsIT (Pixellated Imaging CsI Telescope), made of CsI(Tl) crystals, for high energy. b) Low background counting rate; this has been achieved by optimizing the active and passive shielding and by optimizing the detector configuration via segmentation and 3D capability. c) Position sensitive detector with fine intrinsic spatial resolution coupled with a passive coded mask positioned ~3 m above the detection plane.

The thickness of PICsIT has been chosen in order to optimise the sensitivity at 511 keV, and to ensure a good detection efficiency in the MeV region. The sensitivity of a gamma-ray telescope can be approximated by:

$$S = \text{const.} \times \sqrt{B/A}/\varepsilon, \quad (1)$$

where B is the background count rate, A is the detection area, and ε is the detection efficiency. Assuming B proportional to the volume of the detector (a reasonable approximation in the PICsIT energy range since

the hadronic contribution dominates the background for energies greater than few hundreds keV), equation (1) becomes:

$$S = \text{const.} \times \sqrt{t}/(1 - e^{-\mu t}), \quad (2)$$

where μ is the linear attenuation coefficient of the material (CsI in our case), t is the thickness of the detector, and the constant includes all the other parameters. Fig. 1 (left panel) shows the profile of S as a function of the product μt . The right panel of Fig. 1 shows the optimum thickness as a function of energy, indicating that the optimum thickness for the 500 keV region is slightly less than 3 cm. The value of 3 cm has been chosen in order to maintain a good sensitivity also in the MeV region.

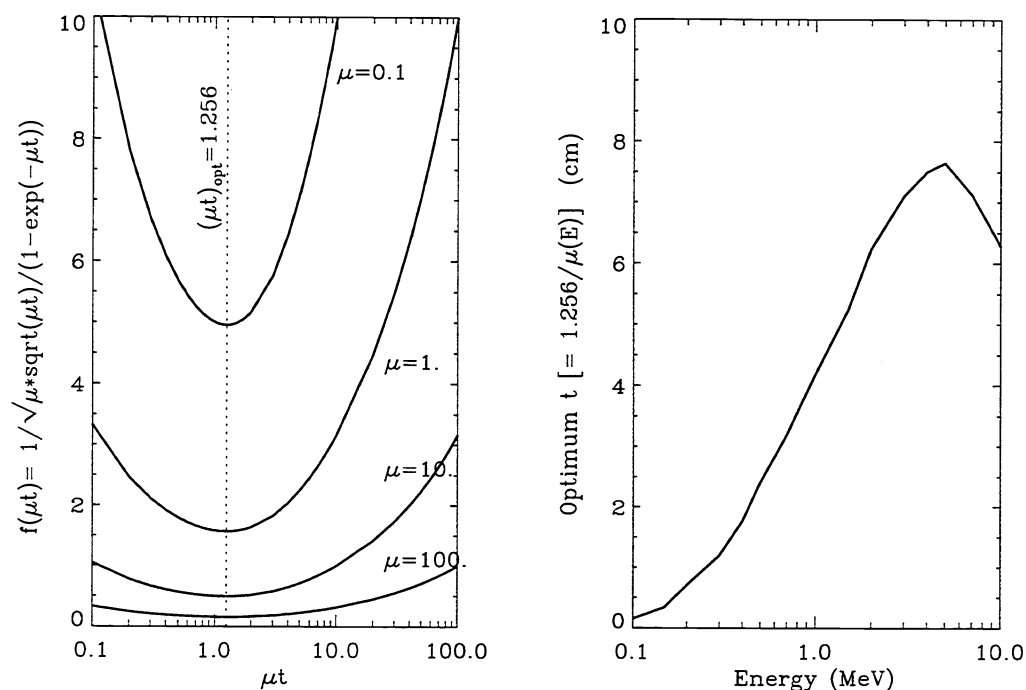


Fig. 1: Optimization of PICsIT thickness. Left panel: best sensitivity as a function of μt (see text) for different values of μ . Right panel: Optimum thickness as a function of energy.

2. PICsIT TECHNICAL DESCRIPTION

The overall PICsIT architecture is depicted in Fig. 2. The requirements for IBIS as a whole are the following:

Weight (max)	628 kg
Power (max)	220 W
Mass memory	2 Mbyte
Telemetry	17-57 kbits/s

In particular the mass and power budgets for PICsIT are 87 kg and 70 W respectively.

The detection plane is made with 8 independent rectangular modules arranged in a 2×4 array, each one containing 512 prisms of CsI(Tl) scintillator crystal. The eight modules are supported by a web structure that

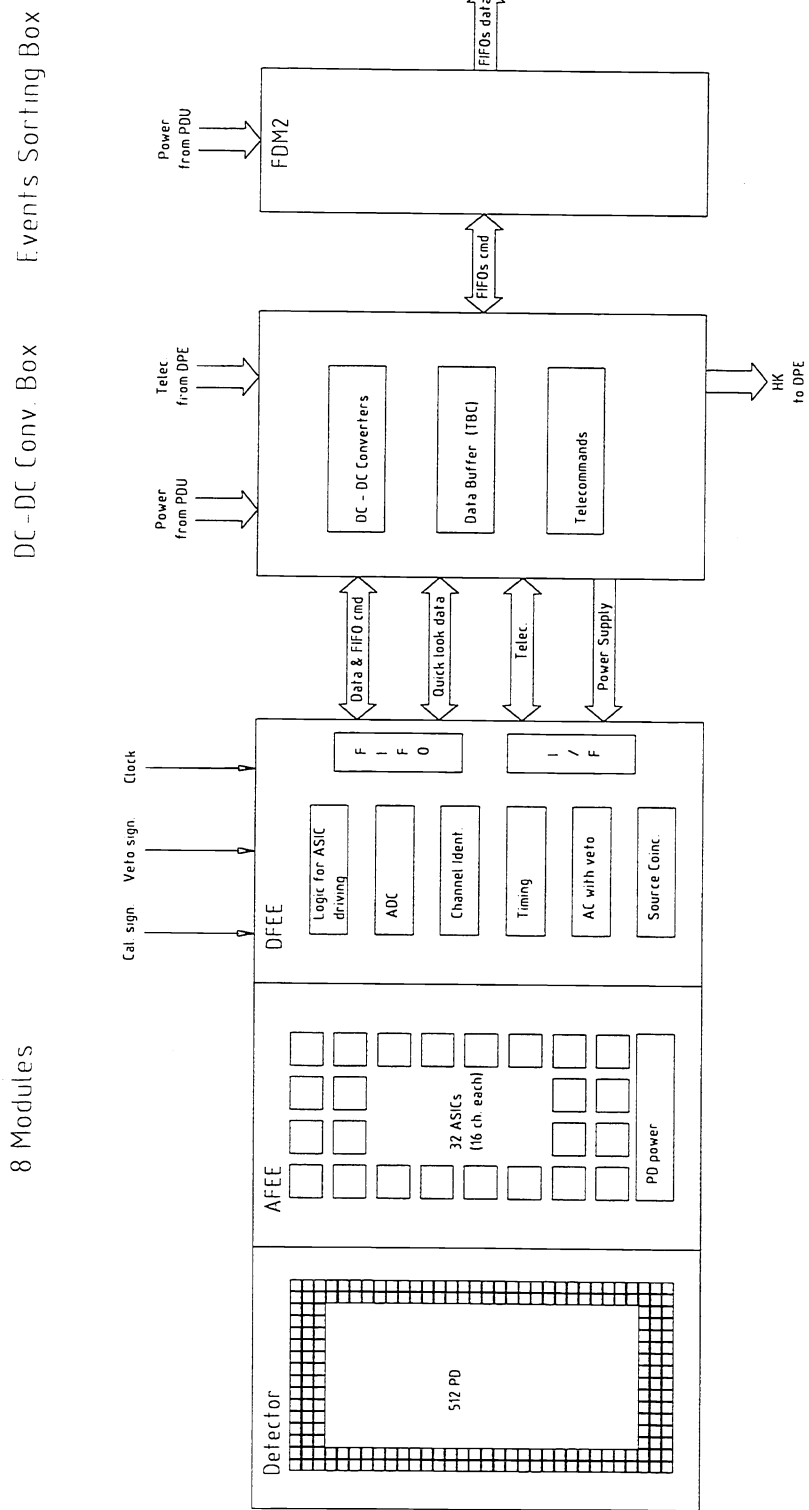


Fig. 2 PICsIT electrical architecture

interfaces PICsIT to IBIS and contains cabling. All the modules are identical, and each one can be assembled and tested independently with a proper test equipment in order to fulfill the requirement of modularity.

For each module, a mechanical egg-crated structure (Fig. 3) with 16×32 holes contains the detection units. The external sides of this structure, made of Aluminium having a thickness equal to half of the pixel size, give mechanical support to the module electronics and for the assembly in the layer. Each crystal is optically glued to Silicon photodiode (PD) to allow for conversion of light pulse in charge. The design foresees two printed circuit boards (PCB) in each module, for analogue and digital front end electronics (AFEE and DFEE).

The first PCB contains the AFEE. It interfaces each PD to a chain including: biasing filter, charge amplifier, shaping amplifier, threshold discriminator and peak detector plus stretcher. Most of these circuits will be implemented in an analogue application specific integrated circuit (ASIC). Each ASIC will serve 16 PDs.

The second PCB is the DFEE. Its main functions are: pixel identification, signal amplitude conversion, signal-veto shield coincidence selection, and event time tagging.

Finally PICsIT includes two external electronics boxes. The first one is devoted to housekeepings, telecommand circuits and the DC/DC converters for the eight modules power supply. The second one contains the circuits for sorting all the CsI events according to their arrival time and for commanding the interfacing process to the data processing electronics (DPE) of IBIS. The timing ordering function is essential to decrease the computing demand in the IBIS DPE. The sorting will be performed by hardware logic.

2.1 Detection unit

The individual detector assembly is depicted in Fig. 4. Each CsI(Tl) crystal has a square cross section of $0.865 \times 0.865 \text{ cm}^2$ and is 3 cm thick. The crystal is polished and wrapped with a white diffusive coating, and optically glued to a custom made low leakage PIN type PD to allow for conversion of light pulse in charge. The detector is forced inside its hole in an Aluminium egg-crated frame that acts also as optical separator between the crystals. An electro-eroding technique is used to work the egg-crated frame, allowing a wall thickness of $200 \mu\text{m}$. The final centre-to-centre distance between pixels is 0.92 cm.

For optical coupling between the PD and the CsI crystal the baseline product is DC-93-500. This is a space-grade silicon rubber with good transparency and adhesion properties. The possibility to hold together PD and crystal permanently before their introduction into the frame simplifies the working procedures for the assembly, and the mechanical design as well.

This detector configuration allows to reach a light yield at PD greater than 30 electrons/keV.

2.2 Analogue front end electronics

The requirements in terms of performance, power consumption, and volume have implied the use of custom designed analogue ASICs to process the PD signal. Each module contains 32 ASIC chips. Fig. 5 shows the block diagram of the AFEE. The ASIC includes 16 signal channels and a read out multiplexer. Each processing channel is made by a low noise charge pre-amplifier followed by a shaping amplifier, sample-and-hold circuit and low-level discriminator. A dedicated digital logic is used to multiplex the output of the analogue data.

Three different phases can be envisaged in the ASIC operation: data capture, data read out, and reset. The signals coming from the RC-CR shaper feed the sample and hold and the discriminator circuit. When any of the discriminator inputs goes over the threshold, the ASIC shall drive the data ready output in its active state and

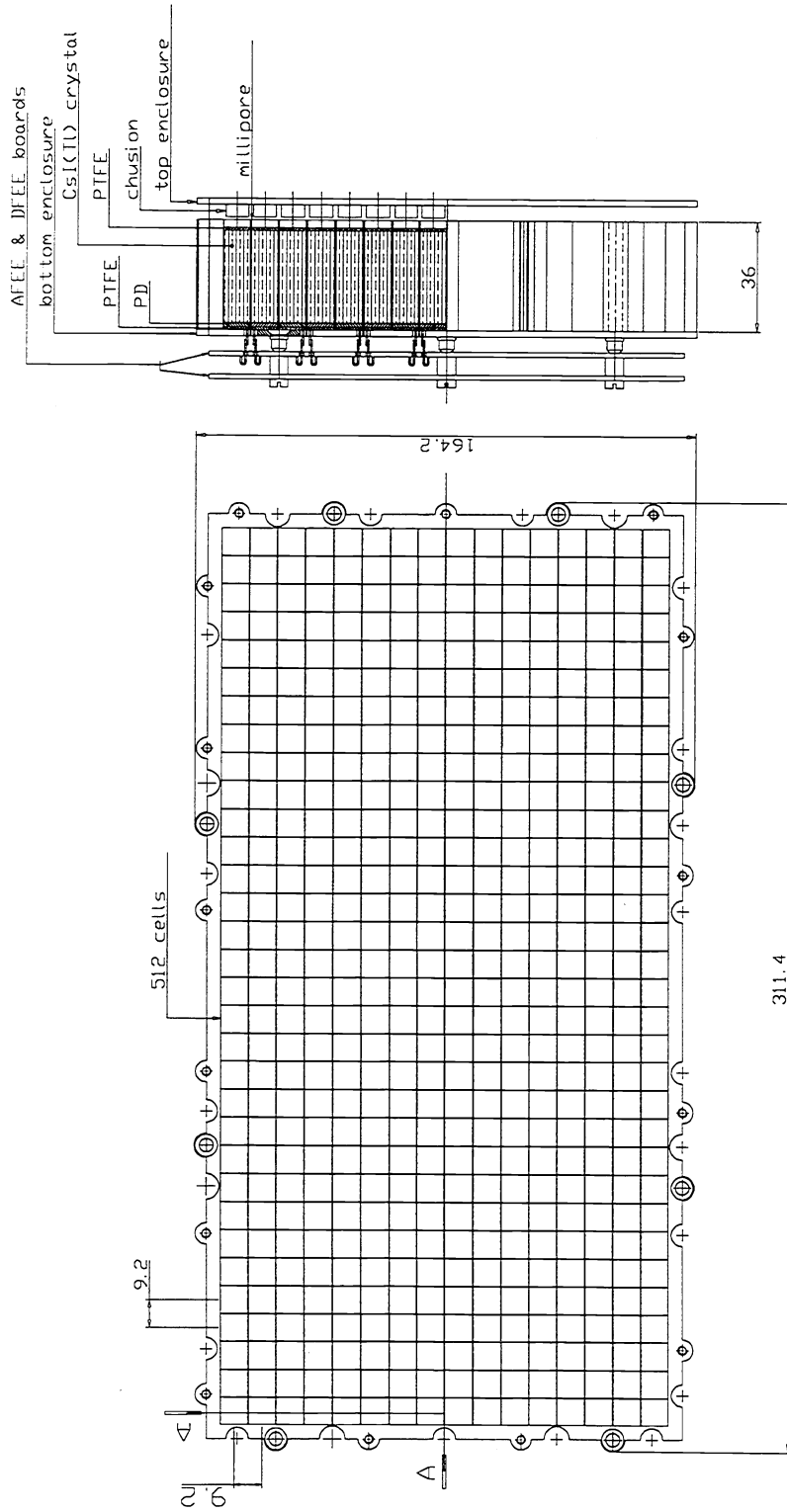


Fig.3 Schematic mechanical design of a PICsIT detection module

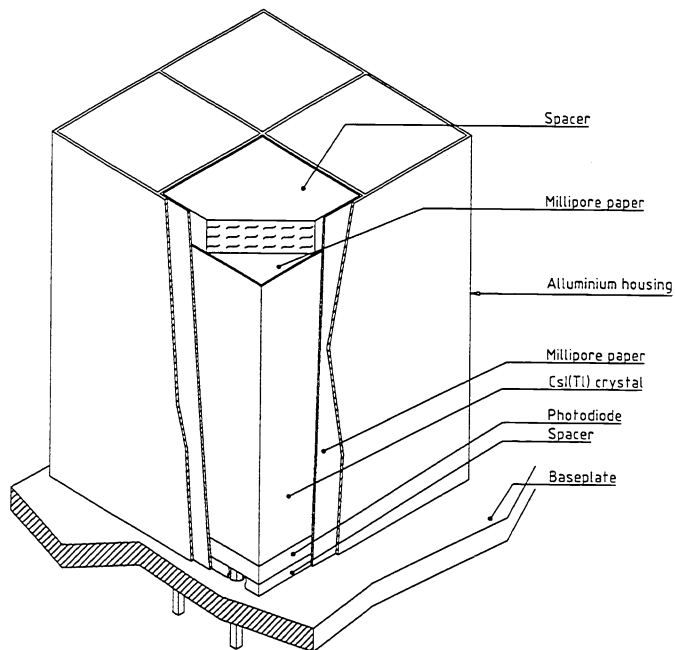


Fig 4 Schematic view of individual pixel detector assembly

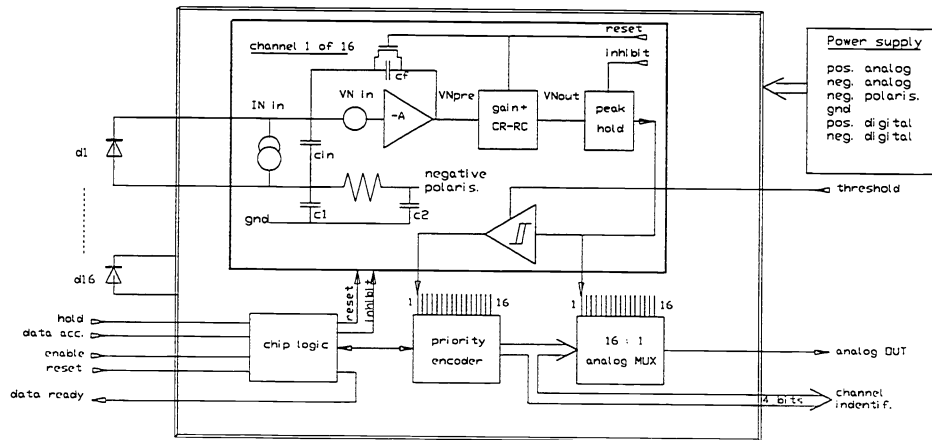


Fig 5 Block diagram of AFEE's (Analogue Front End Electronics) ASIC

inform the external logic about the presence of information inside the chip to be read out. After a fixed time window an hold input should be set in its active state blocking all the ASIC sample and hold discriminators. Channels whose discriminator has been activated are then read out in sequence driving a data accept input to its active state. At the end of the read out process a reset operation is performed to discharge all sample and hold and release discriminator circuits. A calibration input is considered for normal circuit testing operations. The ASIC will have the following characteristics:

Noise (with 50 pF detector, 10 nA leakage current)	600 e ⁻ rms
Max power consumption	8 mW per channel
Max walking time and jitter of the threshold tagging	1 μs
Peaking time	5 μs
Minimum input signal (= 100 keV energy deposit)	3000 e ⁻
Maximum input signal in the linear range	> 1.8 × 10 ⁵ e ⁻
Max threshold difference between channels	±300 e ⁻
Operating temperature range	0–40 °C
Radiation hardness	5 kRad

The ASIC shall also be in accordance with ESA space qualification requirements².

2.3 Digital front end electronics

Each detector module will be provided with a DFEE board placed just under the AFEE one. Each DFEE will be able to perform the following functions:

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- a) Interface to 32 ASICs in the associated AFEE module
 - b) Detect a data ready signal from the module (event has occurred)
 - c) Reset if more the three active pixels are found in the module
 - d) Assigne time of detection to the event
 - e) Identify the ASIC(s) which generated the data ready in the AFEE
 - f) Read out the content of active ASIC(s) searching for active pixel(s)
 - g) Perform A/D conversion of the pulse amplitudes stored in the active pixel(s) in each active ASIC(s)
 - h) Perform, if necessary (depending on the pulse height), event time of detection correction
 - i) Manage active shield veto sytem and calibration source coincidence
 - j) Format output data as: event time, pixel address, pulse amplitude, calibration and multiple conversion flags
 - k) Temporary store output data in a local FIFO
 - l) Manage serial transmission of FIFO data to the DPE unit upon request
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Each DFEE will be also in charge of all auxiliary control functions associated to its AFEE module like threshold level setting, and other tests and controls. The final detailed design of the DFEE is driven by the actual design and performance of the ASIC. Therefore some of the above steps can be accomplished in a different sequence.

Some of the above points need a more detailed description. It has been decided to reject events with multiplicity greater than three (step c) on the basis of MonteCarlo data, which have indicated that the efficiency of these events is less that 3% (see Figure 8).

The action described in point h can derive from the discriminator circuit in the ASIC. In fact, in order to have a low electronic noise, a shaping circuit has been included in the ASIC with an optimum shaping time of 5μsec. If the threshold discriminator circuit in the ASIC is simply made with a level crossing, then the time of

detection of the event will depend from its final amplitude level and will need correction. At this stage of the ASIC realisation it is not sure that this function can be avoided.

Point i takes into account the behaviour of PICsIT when an anticoincidence (AC) event occurs. The accuracy in the time of detection of PICsIT events impacts on the width of the AC time window and hence on the detector dead time. For an expected AC count rate of 30000 counts/s, it is foreseen to constrain the total dead time to less than 5%.

The data stream describing a single event will contain 50 bits.

3. PICsIT EXPECTED PERFORMANCES

3.1 Expected PICsIT count rate

The evaluation of the expected count rate for IBIS is required both for scientific reasons (evaluation of detector sensitivity) and also for the optimization of the resources in the definition of the operational modes, and for the problems associated with the design of the electronics.

The count rate of a shielded detector is in first approximation proportional to the mass, and depends also upon the form factor which for a cylindrical detector of radius r and thickness t is equal: $(\pi r^2 + \pi r t)/2$. The particle orbit environment is also important, especially in the PICsIT energy range, and it varies when going from a low Earth orbit (LEO) to a high eccentric orbit (HEO). The Sun activity, finally, has also an impact. In the HEO scenario, which is currently the baseline for INTEGRAL, the expected proton flux has an increase of a factor of 2 when going from a solar maximum to a solar minimum activity period.

The expected count rate of PICsIT has been calculated both using MonteCarlo simulations, and scaling processes based on geometrical considerations and comparison with data obtained previous high energy space missions. The design of the electronics of PICsIT, and also the definition of its operative modes have been based on the conservative evaluation which is of 7500 counts/s and 15000 counts/s in the case of maximum and minimum solar activity respectively.

3.2 Energy resolution and low energy threshold

The accuracy in the measurement of the signal depends on statistical effects, and on the electronic noise. The number of electron produced follows poissonian statistics, therefore the standard deviation of the signal n is \sqrt{n} . The electronic noise of the read-out system is measured in number, N , of electrons rms equivalent at the PD input. The energy resolution is then given by the following relation:

$$\left(\frac{\Delta E}{E}\right)_{\text{FWHM}} = 2.36 \frac{\sqrt{n + N^2}}{n} \quad (3)$$

N depends on the device characteristics (PD leakage current and capacity) and on the design and technology of the charge pre-amplifier used. With standard pre-amplifier the value of N that can be achieved is less than 500. This electronics, however, cannot be used in PICsIT for reasons of power and size limitations. The electronics which is presently under development has a final goal of $N = 600$. Fig. 6 shows the spectrum obtained for a ^{22}Na source using hybrid pre-amplifiers. A typical value of the energy resolution is 7% at 662 keV.

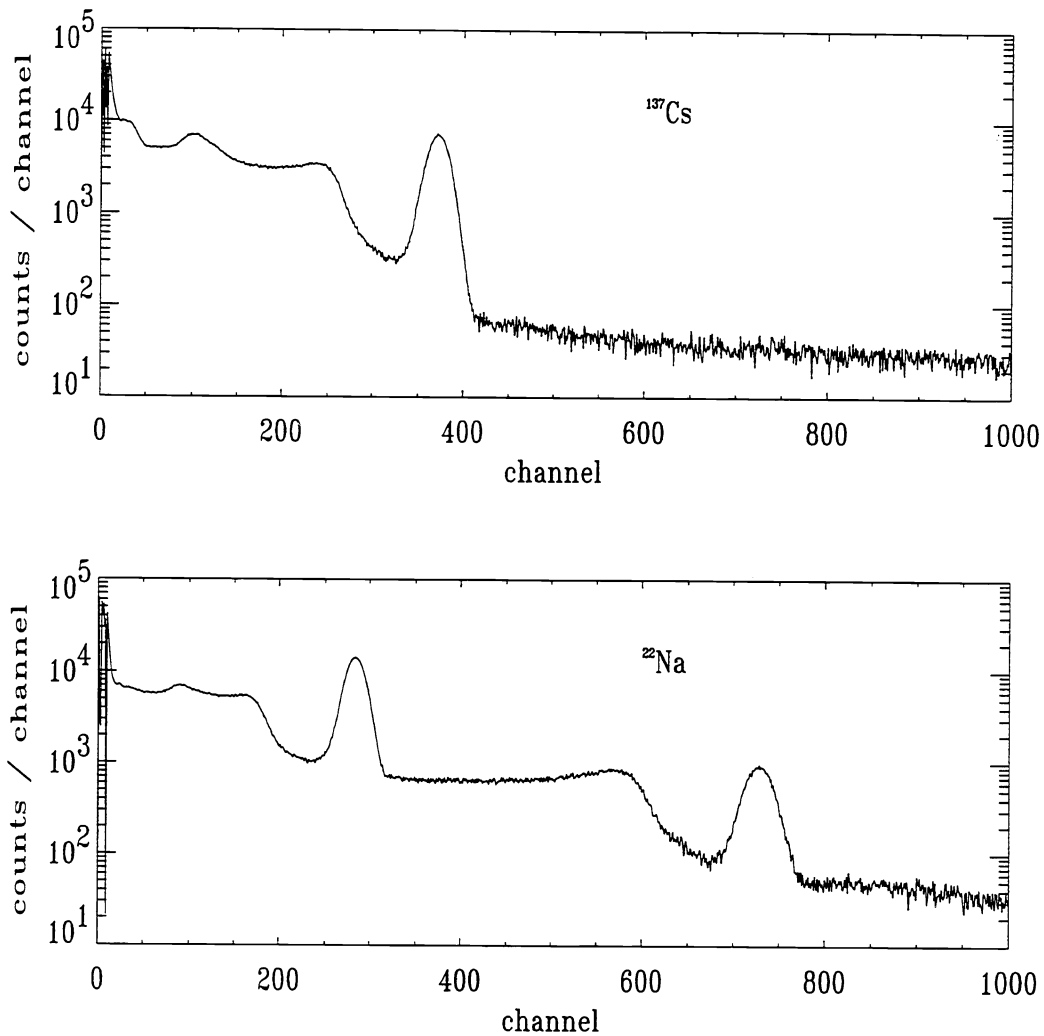


Fig. 6: Count spectra (upper panel: ^{137}Cs source; lower panel: ^{22}Na source) obtained with hybrid preamplifier applied to a CsI(Tl)/PD unit.

The low energy threshold is dependent again on N , as the minimum detectable charge value has to be put at 5σ above the electronics noise. Assuming $N = 600$ then the minimum energy threshold results around 100 keV.

Various measurements have been performed to test the behaviour of the CsI/PD system as a function of the temperature.

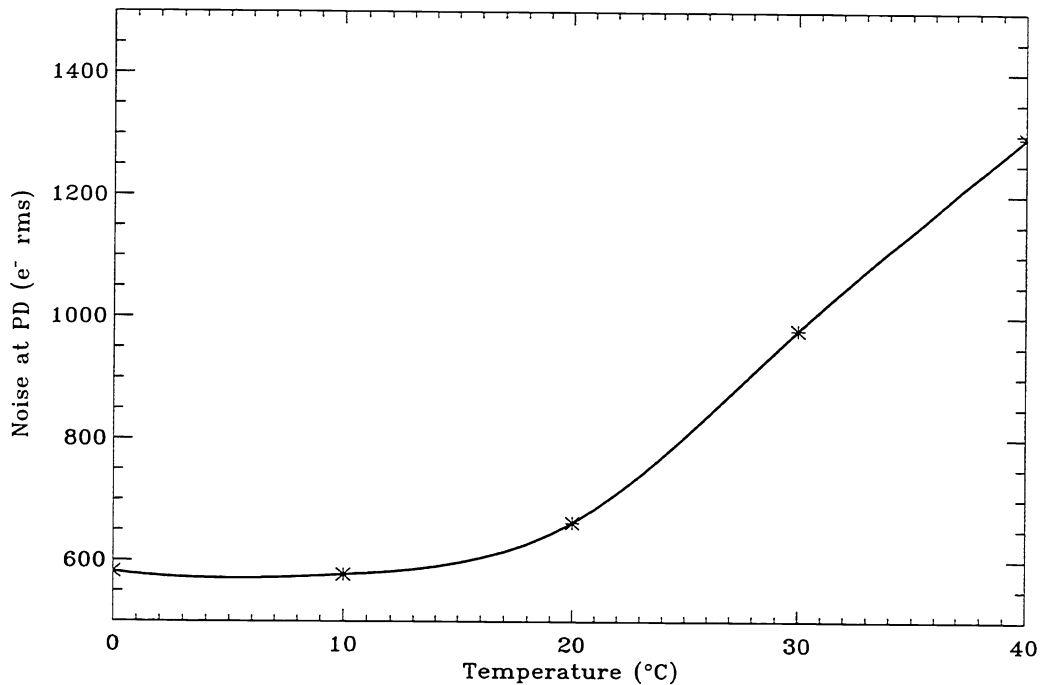


Fig. 7: Noise behaviour as a function of temperature for a CsI(Tl) unit $8 \times 8 \times 8 \text{ cm}^3$ coupled with a 1 cm^2 PD.

The overall behaviour of the noise as a function of temperature is shown in Fig. 7. The acceptable temperature ranges between 0 and 20 °C.

3.3 Detection efficiency and multiplicity

The detection efficiency of PICsIT is limited by three factors. At low energy the electronic noise (see section 3.1) determines the energy threshold. At high energy the design of the FEE of IBIS has implied a constrain on the dynamic range which has caused the introduction of an electronic energy cut off at 5000 keV which has also limited the detection efficiency beyond this energy. This choice has to be finally assessed. Finally, in order to maintain the optimization around 500 keV, and to optimize the design of PICsIT also for the MeV region increasing its stopping power, a natural solution would be to add a second CsI layer. This has not been feasible for reasons of cost and weight.

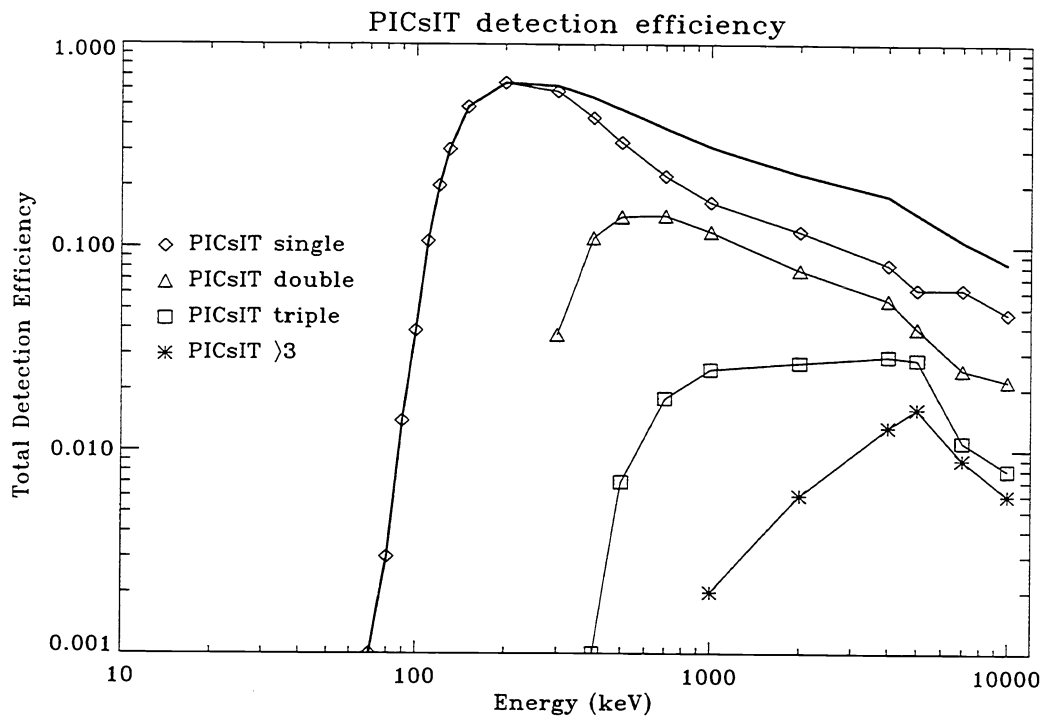


Fig. 8: Total detection efficiency of PICsIT. The curves show the expected efficiency for all events, and for events with multiplicity 1, 2, 3, and greater than 3.

Fig. 8 shows the detection efficiency profile of PICsIT obtained by means of MonteCarlo simulation. The curves for events having multiplicity 1, 2, 3, and >3 are shown.

4. REFERENCES

1. P. Ubertini, these proceedings.
2. F. Lebrun et al. these proceedings.
3. ESA/SCC 9000 Generic Specification.